

What is Claimed:

- 1 1. A bandpass delta sigma truncator comprising:
 - 2 input means for receiving a series of first multi-bit digital signals
 - 3 each having:
 - 4 (a) a number of data bits, and
 - 5 (b) a first number of sign bits;
 - 6 sign extending means for sign extending each of the first multi-bit
 - 7 digital signals to a second multi-bit digital signal having:
 - 8 (a) the same number of data bits as the number of data bits in
 - 9 the first multi-bit digital signals, and
 - 10 (b) a second number of sign bits;
 - 11 output means for supplying from a series of third multi-bit digital
 - 12 signals each individually associated with one of the second multi-bit digital signals
 - 13 and each having the same number of data bits as in an associated second multi-
 - 14 bit digital signal:
 - 15 (a) a series of fourth multi-bit digital signals each having a
 - 16 selected number of the most significant data bits of the third
 - 17 multi-bit digital signals, and
 - 18 (b) a series of fifth multi-bit digital signals each having the
 - 19 remaining number of the least significant data bits of the
 - 20 third multi-bit digital signals;
 - 21 means for:
 - 22 (a) delaying by a period of time equal to the time between
 - 23 successive first multi-bit digital signals each of the fifth
 - 24 multi-bit digital signals, and
 - 25 (b) delaying by a period of time equal to twice the time between
 - 26 successive first multi-bit digital signals each of the fifth
 - 27 multi-bit digital signals and inverting the fifth multi-bit
 - 28 digital signals that have been delayed by a period of time
 - 29 equal to twice the time between successive first multi-bit
 - 30 digital signals;
 - 31 means for multiplying by a multiplier number related to the ratio of
 - 32 a selected frequency to the frequency of the first multi-bit digital signals each of
 - 33 the fifth multi-bit digital signals delayed by a period of time equal to the time
 - 34 between successive first multi-bit digital signals and developing a series of sixth

35 multi-bit digital signals having a number of data bits that is the product of the
36 multiplier number and the number of data bits in the fifth multi-bit digital signals;
37 and

38 summing means for adding to each second multi-bit digital signal:

39 (a) a fifth multi-bit digital signal that has been delayed by a
40 period of time equal to twice the time between successive
41 first multi-bit digital signals and inverted, and
42 (b) a sixth multi-bit digital signal

43 to develop the series of third multi-bit digital signals.

1 2. A bandpass delta sigma truncator according to claim 1

2 wherein:

3 (a) each first multi-bit digital signal is a ten bit digital signal
4 having nine data bits and one sign bit,
5 (b) each second multi-bit digital signal is an eleven bit digital
6 signal having nine data bits and two sign bits,
7 (c) each third multi-bit digital signal is a nine bit digital signal
8 having nine data bits,
9 (d) each fourth multi-bit digital signal is a six bit digital signal
10 having six data bits,
11 (e) each fifth multi-bit digital signal is a three bit digital signal
12 having three data bits,
13 (f) each sixth multi-bit digital signal is a four bit digital signal
14 having four data bits,
15 (g) the multiplier number is 1.75,
16 (h) the selected frequency is 5MHZ, and
17 (i) the frequency of the first multi-bit digital signals is 30MHZ.

1 3. A bandpass delta sigma truncator according to claim 1

2 further including means between said summing means and said output means for
3 determining whether the value of any third multi-bit digital signal is one of:

4 (a) greater than a first value, and
5 (b) less than a second value.

1 4. A bandpass delta sigma truncator according to claim 2

2 further including means between said summing means and said output means for
3 determining whether the value of any third multi-bit digital signal is one of:

4 (a) greater than a first value, and
5 (b) less than a second value.

1 5. A bandpass delta sigma truncator according to claim 2
2 wherein said means for delaying and inverting the fifth multi-bit digital signals
3 include:

4 (a) a digital delay circuit for delaying by a period of time equal
5 to the time between successive first multi-bit digital signals
6 each of the fifth multi-bit digital signals, and
7 (b) a digital delay and inverter circuit for:
8 (1) additionally delaying by a period of time equal to the
9 time between successive first multi-bit digital signals
10 each of the fifth multi-bit digital signals delayed by
11 said digital delay circuit, and
12 (2) inverting the additionally delayed fifth multi-bit
13 digital signals.

1 6. A bandpass delta sigma truncator according to claim 4
2 wherein said means for delaying and inverting the fifth multi-bit digital signals
3 include:

4 (a) a digital delay circuit for delaying by a period of time equal
5 to the time between successive first multi-bit digital signals
6 each of the fifth multi-bit digital signals, and
7 (b) a digital delay and inverter circuit for:
8 (1) additionally delaying by a period of time equal to the
9 time between successive first multi-bit digital signals
10 each of the fifth multi-bit digital signals delayed by
11 said digital delay circuit, and
12 (2) inverting the additionally delayed fifth multi-bit
13 digital signals.

1 7. A method for truncating a multi-bit digital signal comprising
2 the steps of:

3 providing a series of first multi-bit digital signals each having:
4 (a) a number of data bits, and
5 (b) a first number of sign bits;
6 sign extending each of the first multi-bit digital signals to a second
7 multi-bit digital signal having:
8 (a) the same number of data bits as the number of data bits in
9 the first multi-bit digital signals, and
10 (b) a second number of sign bits;

11 adding to each second multi-bit digital signal to develop a series of
12 third multi-bit digital signals each individually associated with one of the second
13 multi-bit digital signals and each having the same number of data bits as in an
14 associated second multi-bit digital signal:

31 developing from the third multi-bit digital signals a series of fourth
32 digital signals each having a selected number of the most significant data bits of
33 the third multi-bit digital signals.

1 8. A method for truncating a multi-bit digital signal according
2 to claim 7 wherein:

3 (a) each first multi-bit digital signal is a ten bit digital signal
4 having nine data bits and one sign bit,
5 (b) each second multi-bit digital signal is an eleven bit digital
6 signal having nine data bits and two sign bits,
7 (c) each third multi-bit digital signal is a nine bit digital signal
8 having nine data bits,
9 (d) each fourth multi-bit digital signal is a six bit digital signal
10 having six data bits,
11 (e) each multi-bit digital signal that has been delayed by a
12 period of time equal to twice the time between successive

13 first multi-bit digital signals and inverted is a three bit digital
14 signal having three data bits,

15 (f) each multi-bit digital signal delayed by a period of time
16 equal to the time between successive first multi-bit digital
17 signals and multiplied by a multiplier number related to the
18 ratio of a selected frequency to the frequency of the first
19 multi-bit digital signals is a four bit digital signal having four
20 data bits.

21 (q) the multiplier number is 1.75,

(h) the selected frequency is 5MHz, and

(I) the frequency of the first multi-bit digital signals is 30MHz.

1 9. A method for truncating a multi-bit digital signal according
2 to claim 7 further including the step of determining whether the value of any thi
3 multi-bit digital signal is one of:

(a) greater than a first value, and

(b) less than a second value.

1 10. A method for truncating a multi-bit digital signal according
2 to claim 8 further including the step of determining whether the value of any thi
3 multi-bit digital signal is one of:

4 (a) greater than a first value, and

5 (b) less than a second value.